AMENDMENT TO THE CLAIMS

Please replace the presently pending claims with the following amended claims:

1.(Currently Amended) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating a reference voltage lower than the main voltage, characterized in that it comprises

~~means of~~ a first transistor connecting the main voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the reference voltage, and which comprises at least a second transistor having a gate connected to the gate of a third transistor mounted as a diode at the reference voltage, the limiting means comprising means of blocking the first transistor when the predetermined voltage is reached, and the blocking means having first and second mirrors connected to each other.

2.(Cancelled)

3.(Currently Amended) Integrated circuit according to claim 1, characterized in that, when the predetermined voltage is reached, the currents circulating in the ~~connecting means~~ first transistor and in the limiting and/or detecting means are comprised in the region of a few dozen μA.

4.(Currently Amended) Integrated circuit according to claim 1, characterized in that the ~~connecting means comprise~~ first transistor comprises a first power transistor.

5.(Previously Presented) Integrated circuit according to claim 4, characterized in that the drain of the first power transistor is connected to the output and its source to the main voltage.

6-9. (Cancelled)

10.(Currently Amended) Integrated circuit according to ~~claim 9~~ claim 1, characterized in that the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking current to the gate of the first power transistor, so as to block it.

11.(Previously Presented) Integrated circuit according to claim 4, characterized in that the gate of the first power transistor is connected to a command input via a fourth transistor.

12.(Currently Amended) Integrated circuit according to ~~claim 10~~ claim 11, characterized in that the fourth transistor is weaker than the transistors of the second mirror, so that the latter imposes its level on the fourth transistor when it delivers the copy of the blocking current.

13.(Original) Integrated circuit according to claim 1, characterized in that the output voltage corresponds to the logic level "1" of a USB connection.

14.(Original) Integrated circuit according to claim 1, characterized in that the reference voltage is used to supply the logic CMOS section of the integrated circuit.

15.(Previously Presented) Integrated circuit according to claim 1, characterized in that the reference voltage and/or the predetermined voltage have the value of 3 V, the main voltage having a value of 5 V.

16.(Currently Amended) Communication module for an integrated circuit comprising means of delivering, on at least one output, a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating a reference voltage lower than the main voltage, characterized in that it comprises

~~means of~~ a first transistor connecting the main voltage to the output, and

means of limiting the voltage on the output at the predetermined output voltage value, which comprises at least a ~~first~~ second transistor having a gate connected to the gate of a ~~second~~ third transistor mounted as a diode at the reference voltage, the limiting means comprising means of blocking the first transistor when the predetermined voltage is reached, and the blocking means having first and second mirrors connected to each other.

17-20.(Cancelled)

21.(Previously Presented) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating a reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output, which comprise a first power transistor, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage,

the limiting means comprising means of blocking the first power transistor when the predetermined voltage is reached,

the blocking means have first and second current mirrors connected to each other,

the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking current to the gate of the first power transistor so as to block it,

the gate of the first power transistor being connected to a command input via a fourth transistor,

the fourth transistor is weaker than the transistors of the second mirror, so that the later imposes its level on the fourth transistor when it delivers the copy of the blocking current.

22-23. (Cancelled)

24.(Previously Presented) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating a reference voltage lower than the main voltage, and comprising:

means of connecting the main voltage on the output and comprising a first power transistor, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the reference voltage, and comprising means of blocking the first power transistor when the

predetermined voltage is reached, the means of blocking comprising first and second current mirrors connected to each other.

25.(Previously Presented) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage and means of generating a reference voltage lower than the main voltage, and comprising:

means of connecting the main voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the reference voltage, and which comprises means of blocking the means of connecting when the predetermined voltage is reached, wherein the means of blocking comprises a first current mirror that delivers a blocking current when the predetermined voltage is reached on the output and a second current mirror that sends a copy of the blocking current to the means of connecting, so as to block the means of connecting.